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# Memristor Emulator Applications Using the MOS-Only Technique

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***Abstract*—The aim of this paper is to present a work towards a MOS transistor memristor emulator. The starting circuit employs an opamp, negative capacitors and loaded with a nonlinear resistor. The final aim is to design a memristor with only MOS transistors which is easily integrable. To implement the negative capacitance several possible potential circuit examples of MOS-Only type are given. These capacitors realize floating negative capacitances and the ac small signal form is shown. Some simulation results are included to verify theory.**

***Keywords—memristor emulation; MOS-only; negative capacitance simulator; two-port network***

## I. INTRODUCTION

The memristor as the fourth fundamental component was initially proposed by Chua in 1971 [1]. This hypothetical element did not attract much attention until a physical nano-element was discovered in HP labs in 2008 and reported in the journal Nature [2]. Since then there is an increasing publications on this element and its emulators [3]–[6]. The memristor is expected to find applications ranging from non-volatile computer memory to chaotic circuit implementations and even synaptic neuron modelling and simulation in brain like computing systems research [7]. They are also candidates as building block for neural networks and therefore attract attention of neural network research community [8]. To enable all these research activities however effective emulators are necessary. These emulators have to be simple yet effective, integrable, low voltage and low power since a very large number of memristors are to be used in some applications. The memristor emulators are usually faster than the $TiO_2$ physical memristor. In general the memristor emulators in the literature fall into two categories. They either directly simulate memristor operation by employing multipliers and integrating components [9]–[12] or they simulate by linear two ports called mutators, loaded by a nonlinear resistor [13]–[16].

The purpose of this work is to design a circuit, which acts like an actual memristor. One representative feature of the memristor is the programmability of the resistance using an externally applied voltage or current. After a new nanoscale device based on crossbar architecture showing memristive behavior was fabricated in 2008, the memristor possesses significant potential for such next-generation nonvolatile memories. However, commercially available memristors are not expected to be available in the near future due to the cost and technical difficulties involved in nanodevice fabrication. Therefore, a replacement that behaves like a real memristor is urgently needed to allow researchers to study the application circuits of memristors. There are several implementations for simulating memristors, however the search for a simple, low power element is still continuing. This paper presents a simple high frequency low power memristor emulator. During the study since the memristor emulator needs floating negative capacitances several negative capacitors are also implemented. They are presented as ac equivalent circuit. They are presented as additional products and with proper biasing circuit they are candidates to solve for many circuit application problems.

## II. THE TRANSMISSION MATRIX CIRCUIT REALIZATION

A two-port network as shown in Fig. 1 may have six representations. Transmission 'a' representation for this two-port network is given as follows:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}. \tag{1}$$

A special two-port network with the following transmission matrix:

$$T = \begin{bmatrix} a_{11} & 0 \\ 0 & a_{22} \end{bmatrix}, \tag{2}$$

is called a M/R mutator and it is especially useful to emulate memristors. If this two-port network is loaded by a nonlinear resistor a memristive one-port is obtained. This matrix represents the constitutive relations $V_1 = dV_2/dt$ and $I_1 = dI_2/dt$.

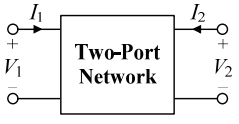


Fig. 1. Two-port network.

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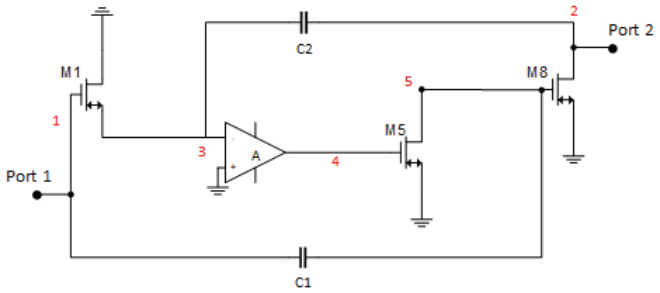



Fig. 2. Emulator circuit ac model.

The corresponding mutator ac model is shown in Fig. 2. Here the MOS transistors ac model is considered to find the mathematical relations. In other words each MOS transistor is a voltage-controlled current source (VCCS) with a certain transconductance $g_m$. Theoretically the MOS transistors can be replaced either by NMOS or PMOS transistor as long as the proper VCCS function is accomplished. In Fig. 2 the dc bias is not shown. For actual operation, all MOS transistors should be biased in saturation. This is obtained by injecting or drawing dc currents to/from appropriate nodes.

This two-port network realizes the transmission matrix given as:

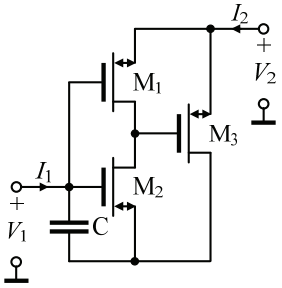
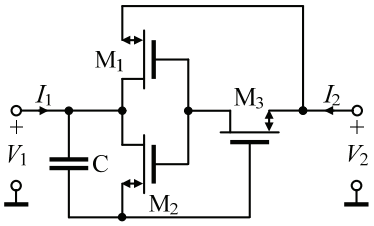
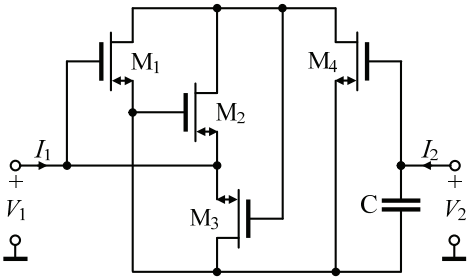
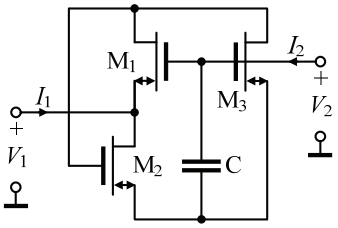
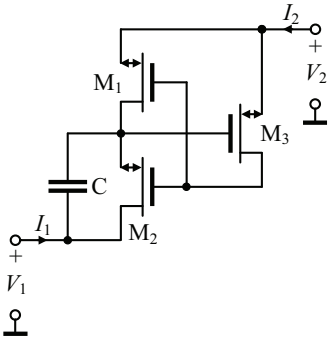
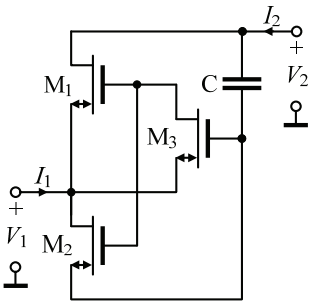
$$T = \begin{bmatrix} \dfrac{sC_1}{g_{m8}} & 0 \\ 0 & -\dfrac{sC_2}{g_{m8}} \end{bmatrix}. \tag{3}$$

According to the transmission matrix, one needs to use a negative capacitor $C_2$ because Eq. (2) and Eq. (3) must be same structure with positive elements. Hence, to make equal $a_{11}$ and $a_{22}$ parameters, we have to use a negative capacitor. Therefore, in the next section we presented several possible new floating negative capacitance simulators that can be used to realize this function.

## III. Implementation of Negative Capacitors

As explained in the previous section the emulator circuit needs a negative capacitor. Hence, we produced 6 different circuits and these circuits are given in tabular form below. The topologies are generated by computer assisted methods. The main idea is to build negative floating capacitance simulators using only transistors. Transistor only circuit idea and several applications are presented in [17]–[19].

TABLE I. Floating Negative Capacitance Simulators (Bias Configuration Not Shown)

| | | |
|---|---|---|
|  |  |  |
| $C_{eq} = -\dfrac{g_{m1}}{g_{m2}} C$ | $C_{eq} = -\dfrac{g_{m1}}{g_{m2}} C$ | $C_{eq} = \dfrac{g_{m1} - g_{m2}}{g_{m1} - g_{m2} + g_{m4}} C$ |
|  |  |  |
| $C_{eq} = -\dfrac{g_{m1}}{g_{m3}} C$ | $C_{eq} = \dfrac{g_{m1}}{g_{m1} - g_{m2}} C$ | $C_{eq} = \left(1 - \dfrac{g_{m1}}{g_{m2}}\right) C$ |

A special case is the MOS-only case, where MOSFETs are used to design circuits and many applications in this area are presented recently [20]–[31]. In the work presented in this paper, for all circuits the ac models are used for calculations and for each of them the MOS transistor works as a VCCS. Proper biasing is needed for functionality.

Biasing for all circuits is not possible within the framework of this study. Moreover, there is no unique design. Each transistor for the circuits in Table I can be selected either as NMOS or PMOS as long as the circuit can be biased properly. The parameters should be selected appropriately to obtain a negative floating resistance. Furthermore some of them can be used as a capacitance multiplier to obtain large capacitors. Note that with proper design all circuits can be used as variable capacitance circuit in form of voltage or current controlled element. Each circuit can potentially be biased after selection of each transistor (NMOS or PMOS) in various ways. An optimization for a best solution is out of the scope of this work.

## IV. Simulation Results

To illustrate memristive operation firstly, ideal circuit elements are used for the circuit in Fig. 2. Instead of transistor, voltage controlled current source is used and instead of opamp, voltage controlled voltage source is inserted.

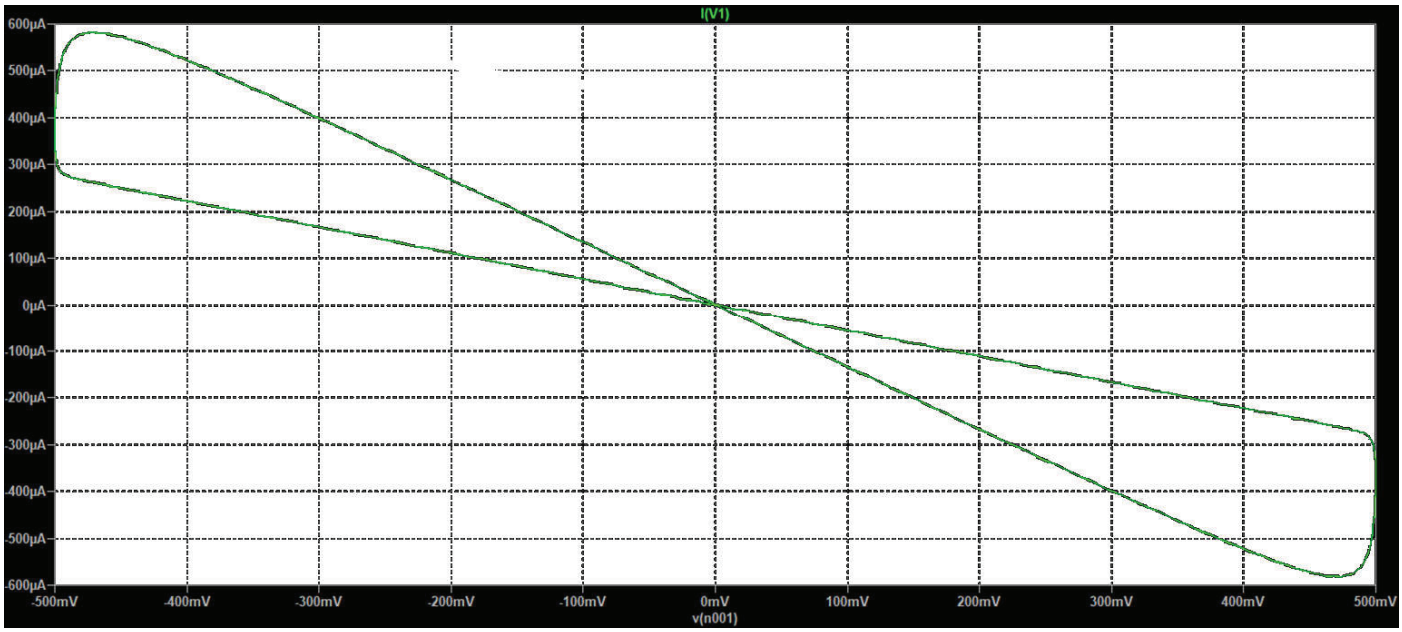



Fig. 3. Voltage-current characteristics of ideal emulator.

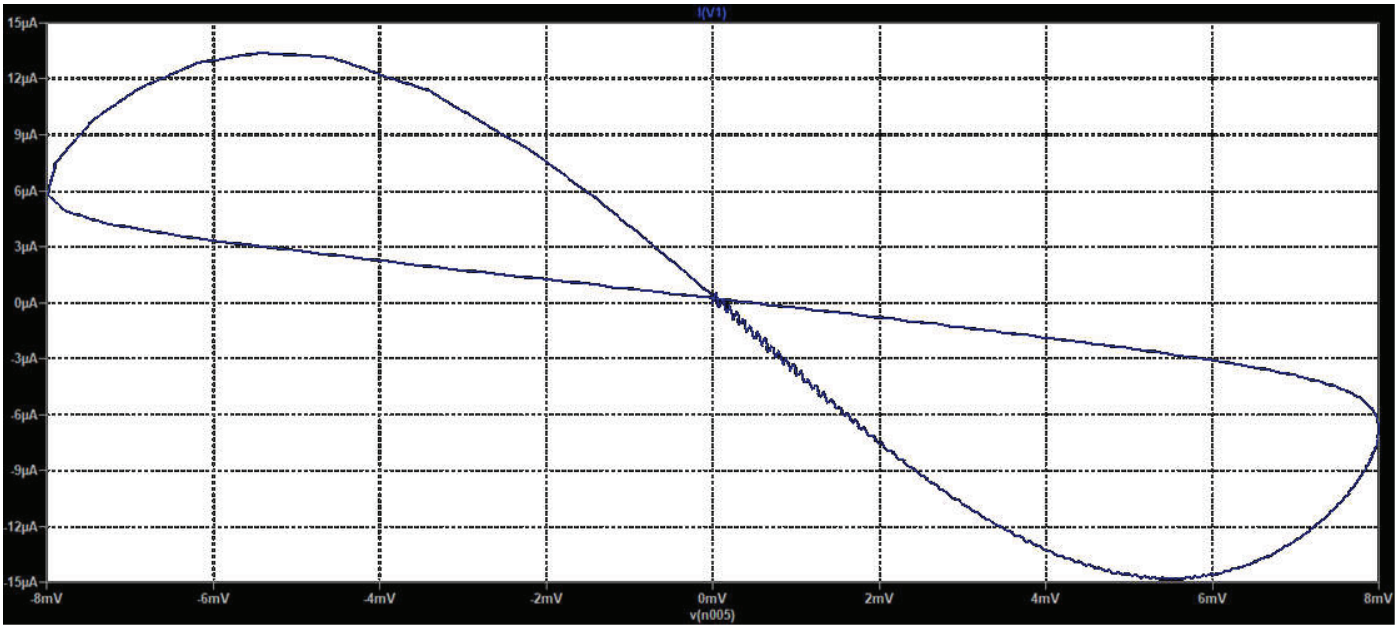



Fig. 4. Voltage-current characteristics of non-ideal emulator ($V_{in}$ = 8 mV).

Figure 3 shows the expected memristive behaviour. For simulation, $C_1 = 300$ nF and $C_2 = -300$ nF values are used. Port 2 is loaded with a diode in series with a 1.2 kΩ resistor and this combination in parallel with 1.8 kΩ resistor to simulate a nonlinear resistor. As a next step we replaced VCCSs with transistors and we obtained the voltage-current characteristic as shown in Fig. 4. For performance optimization further work is needed. From the figures one can observe the resistance change in forward and reverse paths which is the characteristic behaviour of memristive operation and is called pinched hysterisis loop.

## V. CONCLUSION

In this paper, a work towards an integrable memristor emulator is presented. The negative capacitances in the circuit can easily be simulated with integrable MOS-only type floating capacitance simulators which are given in tabular form. An optimized MOS-only type memristor emulator is a future study. However, the aim of the presented material is to illustrate the integrable, low power MOS design possibilities of memristors. Moreover six new floating negative capacitance simulators are presented which obviously have applications beyond memristor emulation. Some simulation results are also included to verify theory.

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